MIC0013-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: TZU YU WANG	)	Confirmation No. 1061
	)	
Serial No: 10/656,224	)	Art Unit: 2823
	)	
Filed: September 8, 2003	)	Examiner: Brook Kebede
	)	
Title: METHOD FOR SUPPRESSING BORON PENETRATION BY IMPLANTATION IN P+ MOSFETS	)	

SUBMISSION OF REVOCATION OF POWER OF ATTORNEY AND GRANT OF POWER OF ATTORNEY

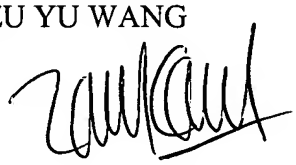
Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit the attached Revocation of Power of Attorney and Grant of Power of Attorney in the above-identified application. Should there be any questions with respect to this submission a representative of the Patent Office is requested to contact the undersigned.

Respectfully submitted,

TZU YU WANG



Date: February 10, 2005 By: _____

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Customer No. 28970

PATENT
Customer No. 28970

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Application and Patent Numbers: See attached "Schedule A"

REVOCATION OF POWER OF ATTORNEY
AND GRANT OF NEW POWER OF ATTORNEY

The undersigned, a representative authorized to sign on behalf of the assignee owning all of the interest in the listed and pending patent applications and issued patents on the attached sheet (Schedule A), hereby revokes all previous powers of attorney or authorization of agent granted in these patents before the date of execution hereof and appoints all the attorneys associated with Customer Number 28970.

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Date: January 10, 2005

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By: Billie Chen
Name: Billie Chen
Title: Director of IP & Legal Office

SCHEDULE A

SERIAL NUMBER	FILING DATE	TITLE	PATENT NUMBER	ISSUE DATE
10/237,668	9/10/2002	Ono Interpoly Dielectric Flor Flash Memory Cells and Method for Fabricating The Same Using a Single Wafer Low Temperature Deposition Process	6,777,764	8/17/2004
10/230,328	8/29/2002	Method for Removing Fences Without Reduction of Ono Film Thickness	6,677,255	1/13/2004
10/230,666	8/29/2002	Programming A Flash Memory Cell	6,760,257	7/6/2004
10/426,833	5/1/2003	Apparatus and Method for Inhibiting Dummy Cell Over Erase	6,787,860	9/7/2004
10/076,629	2/19/2002	Protection Layer to Prevent Under-Layer Damage During Deposition	6,573,177	6/3/2003
10/151,150	5/21/2002	Sensing Method for EEPROM Refresh Scheme	6,639,839	10/28/2003
10/101,930	3/21/2002	Semiconductor Device with Minimal Short-Channel Effects and Low Bit-Line Resistance	6,555,844	4/29/2003
10/101,922	3/21/2002	Sonos Component Having High Dielectric Property	6,498,377	12/24/2002
10/101,931	3/21/2002	Method for Forming An Oxide Layer on a Nitride Layer	6,551,879	4/22/2003
10/186,619	7/2/2002	Structure for Preventing Salicide Bridging and Method Thereof	6,677,199	1/13/2004
10/132,286	4/26/2002	Method of Preventing Tungsten Plugs From Corrosion	6,703,301	3/9/2004
10/197,896	7/19/2002	Method for Forming A Phase Change Memory	6,759,267	7/6/2004
10/214,770	8/9/2002	Memory Device and Operation Thereof	6,788,602	9/7/2004
10/847,277	5/17/2004	Method for Forming A Phase Change Memory	N/A	NA
10/176,065	6/21/2002	Neural Network for Determining the Endpoint in a Process	N/A	NA
10/387,489	3/14/2003	Photoresist Pump Dispense Detection System	N/A	NA
10/439,014	5/16/2003	Cleaning Systems With Monitaring Functions	N/A	NA
10/600,700	6/23/2003	Peer Version Control System	N/A	NA
10/667,447	9/23/2003	Batch Order Change System	N/A	NA
10/733,230	12/12/2003	Elimination of the Fast-Erase Pheonomena in Flash Memory	N/A	NA
10/731,150	12/10/2003	Cleaning Method Using Ozone DI Process	N/A	NA
10/685,484	10/16/2003	Endpoint Detection in Manufacturing Semi-Conductor Device	N/A	NA

SERIAL NUMBER	FILING DATE	TITLE	PATENT NUMBER	ISSUE DATE
10/857,866	6/2/2004	Program/Erase Method for P-Channel Charge Trapping Memory Device	N/A	NA
10/465,852	6/20/2003	Method for Reducing Dimensions Between Patterns on a Hardmask	N/A	NA
10/739,049	12/19/2003	Method for Reducing Dimensions Between Patterns on a Photoresist	N/A	NA
10/673,359	9/30/2003	Structure for Preventing Salicide Bridging and Method Thereof	N/A	NA
10/873,142	1/14/2004	Non-Volatile Memory Cell and Operating Method	N/A	NA
10/237,082	6/2/2003	Memory Device With Built-In Error-Correction Capabilities	N/A	NA
10/449,590	6/2/2003	Memory Device With Built-In Error-Correction Capabilities	N/A	NA
10/361,681	2/11/2003	Semi-Conductor Device With Minimal Short-Channel Effects and Low Bit-Line Resistance	N/A	NA
10/715,558	11/19/2003	Method of Forming a Polysilicon Layer Compressing Microcrystalline Grains	N/A	NA
10/414,048	4/16/2003	ONO Dielectric for Memory Cells	N/A	NA
10/418,121	4/18/2003	Method of Integrating The Fabrication Process for Integrated Circuits and Mem Devices	N/A	NA
10/387,487	3/14/2003	Method for Controlling a Butterfly Valve	N/A	NA
10/653,892	9/4/2003	A Non-Volatile Flash Memory	N/A	NA
10/703,453	11/10/2003	Fabrication Method of Sub-Resolution Pitch for Integrated Circuits	N/A	NA
09/978,546	10/18/2001	Method for Reducting Dimensions Between Patterns on a Photoresist	N/A	NA
10/177,145	6/24/2002	Method for Eliminating Standing Waves in a Photoresist Profile	N/A	NA
10/241,486	9/12/2002	Method for Detecting Solvent Leakage During Manufacture of a Semi-Conductor Device	N/A	NA
10/223,327	8/20/2002	Memory Device and Method of Manufacturing The Same	N/A	NA
10/376,225	3/3/2003	Method of Fabricating ONO Dielectric for Non-Volatile Memories	N/A	NA
10/387,488	3/14/2003	Method of Forming An Embedded ROM	N/A	NA
10/681,099	10/9/2003	Defect Reduction Using Pad Conditioner Cleaning	N/A	NA

SERIAL NUMBER	FILING DATE	TITLE	PATENT NUMBER	ISSUE DATE
		Method of Preventing Over-Erase of Memory Devices		
10/176,061	6/21/2002	Method for Eliminating Standing Waves in a Photoresist Profile	N/A	NA
10/076,630	2/19/2002	Self-Aligned Patterning in Dual Damascene Process	N/A	NA
10/137,406	5/3/2002	Method for Forming Tungsten Plugs to Prevent Corrosion Complexity	N/A	NA
10/186,892	7/2/2002	Method for Forming Self-Aligned Salicides	N/A	NA
10/210,032	8/2/2002	Method for Reduced Photoresist Usage	N/A	NA
10/403,060	4/1/2003	Method of Forming Self-Aligned Contracts	N/A	NA
10/656,224	9/8/2003	Method for Suppressing Boron Penetration by Implantation in P* Mosfets	N/A	NA
10/756,777	1/14/2004	Non-Volatile Memory Cell and Operating Method	N/A	NA
60/390,183	6/21/2002	Sub-90nm Space and Hole Patterning Using 248nm Lithography with Plasma-Polymerization Coating	N/A	NA
		Method for Eliminating Polycide Voids Through Nitrogen Implantation	N/A	NA
10/465,848	6/20/2003	Method for Reducing Dimensions Between Patterns on a Photomask	N/A	NA
10/417,105	4/17/2003	Method of Modulating Threshold Voltage of a Mask ROM	N/A	NA
10/385,483	3/12/2003	Method for Forming Shallow Trench Isolation With Control of Bird Beak	N/A	NA
10/376,229	3/3/2003	Method for Plymer Removal After an Etching Process	N/A	NA
10/465,850	6/20/2003	Method for Shrinking Dimensions of Photoresist	N/A	NA
10/315,003	12/10/2002	Method and System for Lithography Using Phase-Change Material	N/A	NA